IN THE CLAIMS

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A method for supporting software pipelining, comprising:

receiving a shift mask signal having information on a shifting region of a register file;

receiving a shift signal to trigger a shift;

identifying a shifting register queue based on the shift mask signal, wherein the shifting register queue ~~comprising~~ comprises a plurality of queue registers; and

shifting the contents of the queue registers based on the shift signal.

2. (Currently Amended) The method of Claim 1, wherein the ~~receiving the~~ shift mask signal ~~comprising receiving the shift mask signal~~ is received from a shift mask register associated with the shifting register queue.

3. (Currently Amended) The method of Claim 1, wherein ~~receiving the shift signal comprising receiving~~ the shift signal is received from an external component.

4. (Currently Amended) The method of Claim 1, wherein ~~the shifting register queue part of a register file,~~ the register file comprises ~~comprising having~~ the plurality of queue registers and [[comprising]] a plurality of non-queue registers, and wherein the shift mask signal comprises ~~comprising~~ a plurality of bits, each bit associated with a corresponding register in the register file.

5. (Currently Amended) The method of Claim 4, wherein the bits in the shift mask signal that comprise 1s correspond ~~corresponding~~ to the queue registers ~~comprising 1s~~, and wherein the bits in the shift mask signal that comprise 0s correspond ~~corresponding~~ to the non-queue registers ~~comprising 0s~~.

6. (Currently Amended) The method of Claim 4, wherein the bits in the shift mask signal that comprise 0s correspond ~~corresponding~~ to the queue registers ~~comprising 0s~~, and wherein the bits in the shift mask signal that comprise 1s correspond ~~corresponding~~ to the non-queue registers ~~comprising 1s~~.

7. (Currently Amended) A system for supporting software pipelining[[,]] comprising:

a register file comprising:

a plurality of ~~registers, the registers comprising~~ queue registers forming a shifting register queue based on a shift mask signal having information on a shifting region of the register file; and

at least one non-queue register ~~registers, the queue registers forming a shifting register queue, at least one non-queue register~~ located between two queue registers.

8. (Original) The system of Claim 7, further comprising a shift mask register operable to identify the queue registers within the register file.

9. (Currently Amended) The system of Claim 8, wherein the shift mask register is further operable to provide [[a]] the shift mask signal to the register file~~, the shift mask signal operable~~ to identify the queue registers for the register file.

10. (Currently Amended) The system of Claim 7, wherein the register file further comprises ~~comprisesing~~ :

write decoding logic operable to generate control signals and write signals; and

a plurality of multiplexers, ~~the write decoding logic operable to generate control signals and write signals~~, wherein each multiplexer corresponds ~~correspondsing~~ to a register within the register file~~, each multiplexer~~ and is operable to receive one of the control signals from the write decoding logic and is further operable to provide write data to the corresponding register based on the control signal.

11. (Currently Amended) The system of Claim 10, wherein the registers within the register file comprises ~~comprising~~ edge-triggered flip-flops~~, each register~~ and are operable to receive the write data from the multiplexer and to receive one of the write signals from the write decoding logic.

12. (Currently Amended) The system of Claim 11, wherein for each register other than a first register, the write data provided by each multiplexer to the corresponding register based on the control signal comprises ~~comprisesing~~ data from a previous register in the register file.

13. (Currently Amended) A system for supporting software pipelining[[,]] comprising:

a register file ~~comprising a plurality of registers, the register file~~ operable to receive a shift mask signal and a shift signal, to identify a shifting register queue having a plurality of queue registers within the register file based on the shift mask signal, ~~the shifting register queue comprising a plurality of queue registers~~, and to shift the contents of the queue registers based on the shift signal.

14. (Original) The system of Claim 13, further comprising a shift mask register operable to identify the queue registers within the register file.

15. (Currently Amended) The system of Claim 14, wherein the shift mask register is further operable to provide the shift mask signal to the register file.

16. (Currently Amended) The system of Claim 13, wherein the shift mask signal comprises ~~comprisesing~~ a plurality of bits, wherein each bit is associated with a corresponding register in the register file.

17. (Currently Amended) The system of Claim 13, wherein the register file further comprises ~~comprising~~:

write decoding logic operable to generate control signals and write signals; and

a plurality of multiplexers, ~~the write decoding logic operable to generate control signals and write signals,~~ wherein each multiplexer ~~corresponding~~ corresponds to a register within the register file~~, each multiplexer~~ and is operable to receive one of the control signals from the write decoding logic and to provide write data to the corresponding register based on the control signal.

18. (Currently Amended) The system of Claim 17, wherein the registers within the register file comprises ~~comprising~~ edge-triggered flip-flops, and wherein each register is operable to receive the write data from the multiplexer and to receive one of the write signals from the write decoding logic.

19. (Currently Amended) The system of Claim 18, wherein for each register other than a first register, the write data provided by each multiplexer to the corresponding register based on the control signal comprises ~~comprising~~ data from a previous register in the register file.

20. (Currently Amended) The system of Claim 13, wherein the register file is operable to receive the shift signal from an external component.